DESIGN AND DEVELOPMENT OF A 2-COLOR INFRARED EMITTER ARRAY SYSTEM

by

Robert Charles Rehrig

A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering

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Robert Charles Rehrig

Approved: _____

Fouad E. Kiamilev, Ph.D.
Professor in charge of thesis on behalf of the Advisory Committee

Approved: _____

Kenneth E. Barner, Ph.D.
Chair of the Department of Electrical and Computer Engineering

Approved: _____

Babatunde A. Ogunnaike, Ph.D.
Interim Dean of the College of Engineering

Approved: _____

Charles G. Riordan, Ph.D.
Vice Provost for Graduate and Professional Education

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ABSTRACT

Infrared (IR) detectors have a wide array of uses because they can detect what our eyes cannot. We use IR information in astronomy for detecting hidden objects, wireless communication, weather forecasting, and much more. The military also uses infrared detectors for night vision, targeting, and even object tracking. Infrared is popular for object detection because most objects produce thermal frequencies in the IR range. That means with an infrared detector it is easy to observe and characterize an object based on the heat it produces.

Unfortunately, these systems are not always easy to test. The best way to find out if the infrared detector is working is by testing it in the field, which can be expensive and hard to do. Fortunately, there is another way to test these systems that is much safer and more reasonable. It is possible to create an emulation environment so that the sensor can react as if it is in a live situation. This requires an array of IR pixels to reproduce previously observed heat signatures and a projection system to broadcast the array in order for the infrared detector to experience the output as if it were a real event.

Previous work has included creating a 512x512 array of super-latticed LEDs (SLEDS) with one color, but in order to get a better sense of what an incoming object might be, multi-wavelength detection is necessary. The following paper outlines the work completed to create a 512x512 array of SLEDS with two different frequencies instead of one.

Chapter 1

INTRODUCTION

1.1 Background

Infrared (IR) detectors have a wide array of uses because they can detect what our eyes cannot. We use IR information in astronomy for detecting hidden objects, wireless communication, weather forecasting, and much more. The military also uses infrared detectors for night vision, targeting, and even object tracking. Infrared is popular for object detection because most objects produce thermal frequencies in the IR range. That means with an infrared detector it is easy to observe and characterize an object based on the heat it produces.

Testing these infrared detectors can often be difficult to test and characterize without first calibrating. In order to calibrate the system, a large array of pixels is used as a frame of reference, and as the detectors gain higher resolution, the array of pixels also needs to grow in size. In order to achieve greater accuracy, multiple pixel colors can be used to emulate more exact heat signatures.

Previous work has included the development, production, and testing of a single-color 512x512 array of super-latticed light emitting Diodes (SLEDS) documented by Corey Lange, and a 68x68 array documented by Rodney McGee[1][2].

The following paper is a description of the work completed to create a full system for driving and characterizing a 512x512 array of 2-color SLEDS at cryogenic temperatures. The biggest difference between the current array of SLEDS and the previous designs is the additional IR LED in order to produce a larger range of wavelengths. This paper will also outline techniques for designing the 2-color chip, as well as methods used to improve yield.

1.2 Motivation

The SLEDS project has been in motion for many years, and a 2-color design is the next step in developing a system for testing and calibrating infrared detectors. With successfully producing a 512x512 single color array, the next step is to increase the number of pixel colors in order to create a more realistic simulation environment.

The motivation behind the 2-color layout is to improve IR detector precision. With a larger number of test wavelengths, a detector can be calibrated and tested for higher accuracy and precision.

This chip provides an opportunity to improve the current SLEDS design so that it will still fit within the 48 micron dimensions. The more compact design will be combined with new techniques to increase the yield as well. Those methods are currently being developed and will be outlined later in the paper.

Chapter 2

PREVIOUS WORK

2.1 1-Color Design

Up until now, the SLEDS designs have all been for a single-color pixel array. The previous two designs involved a 68x68 array and a redesigned 512x512 array, which featured improvements and expansions over the 68x68 array, as well as a smaller size and additional pins to make testing easier.

2.1.1 68x68 SLEDS array

As documented in Rodney McGee's Master Thesis, Jeremy Ekman and Josh Kramer designed the pixel driver in 2006[2]. The goal of the project was to create an arbitrary subset of LEDs in a two-dimensional array that could be programmed with an analog current. Design specifications included a 1-100mA drive current with a 6.5V bias in a minimum of a 64x64 array. It also need to be possible to turn on up to 10% of the pixels at a given time.

In order to achieve this goal, a new strategy was used that included using IBM 0.13μm SiGe 8HP 200GHz technology, which was uncommon to be used with LED drives. This technology contained seven layers of metal, instead of the four, to allow faster speeds, featured a copper interconnect current density of 5mA/mm^2, and used an NPN design that had a current capacity of 12mA/mm^2, instead of the typical 1.2mA/mm^2 for an NPN transistor.

The outcome was a 68x68 unit cell array with a 120μm unit cell pitch including both metaloxidesemiconductor field-effect transistor MOSFETS and Bipolar transistors, as shown in figure 2.1 and figure 2.2. Due to all of the above, it was possible to design a driver with multiple channels and a current carrying capacity of several amps.

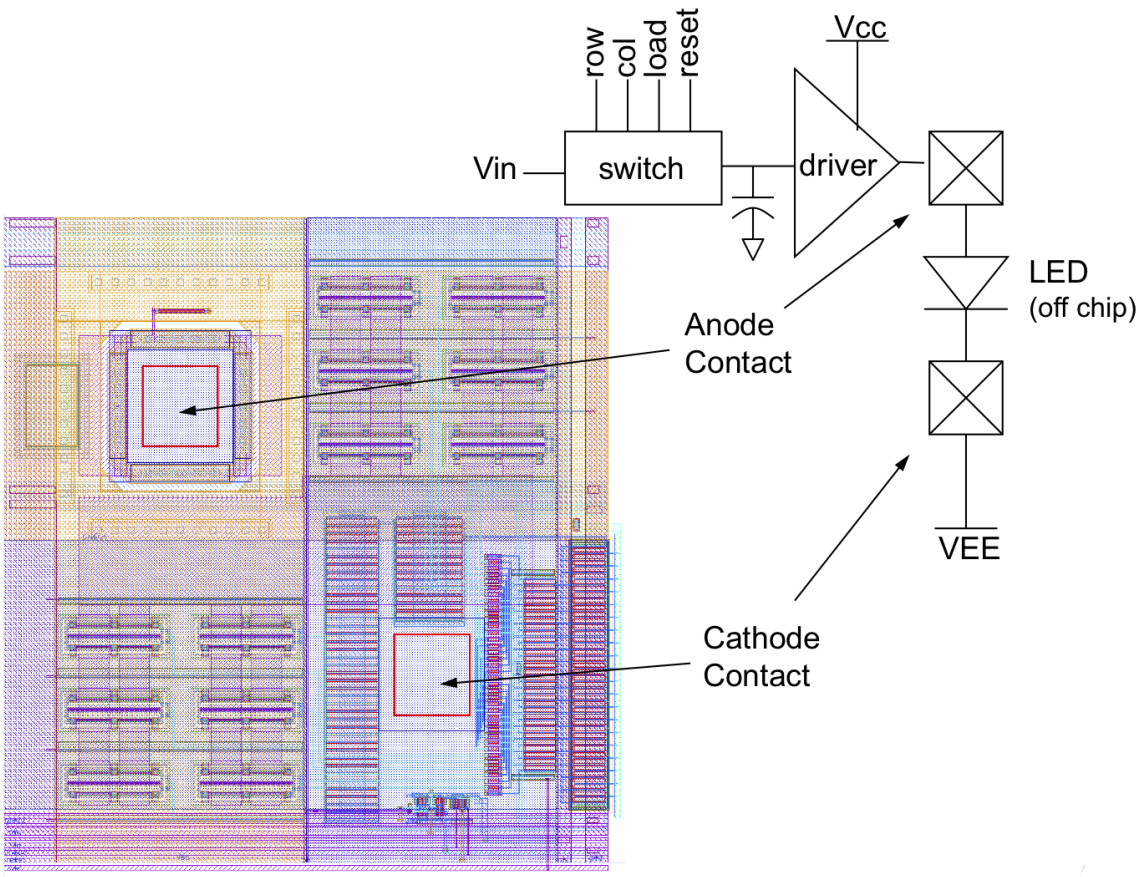


Figure 2.1: 68x68 Unit cell schematic

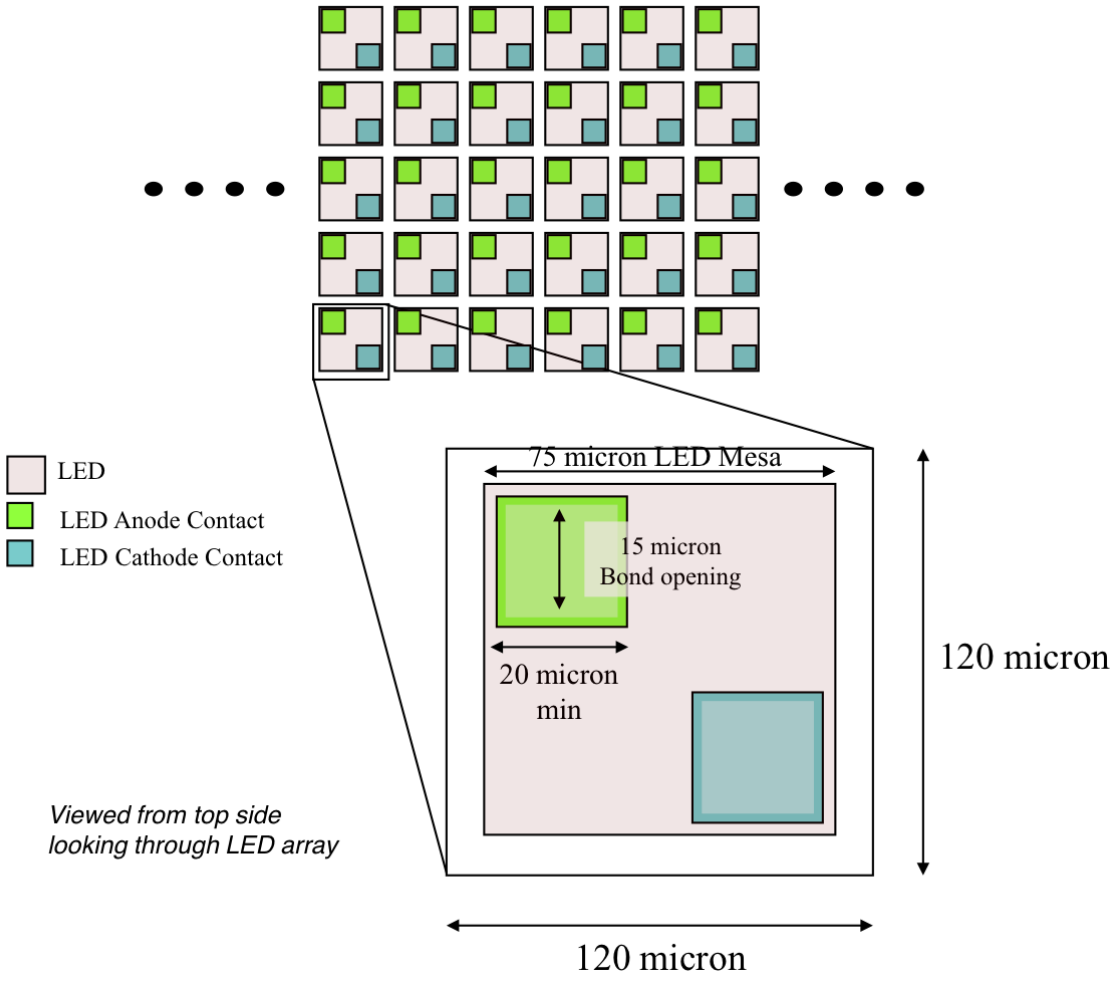


Figure 2.2: 68x68 SLEDS array structure

2.1.2 512x512 SLEDS array

The 512x512 SLEDS pixel array was documented in 2011 by Corey Lange for his Master's thesis[1]. The driver was redesigned for the new array and featured a switch over to a CMOS-only structure, which lead to improvements over the previous 68x68 layout as well as a decrease in the array size. The goal of this chip was to focus on creating a better voltage swing for the pixel, while still maintaining adequate current.

By using a CMOS-only design, changes to the pixel design were made so that the pixel would turn fully on at 0V and fully off at 12V. This is achieved by using P-type MOSFETs (PMOS) for low voltage control and N-type MOSFETs (NMOS) for high voltage control. Using both together in parallel, as shown in figure 2.3, is known as a CMOS pair, and it is useful because it allows full 12V and 0V to be passed to the LED.

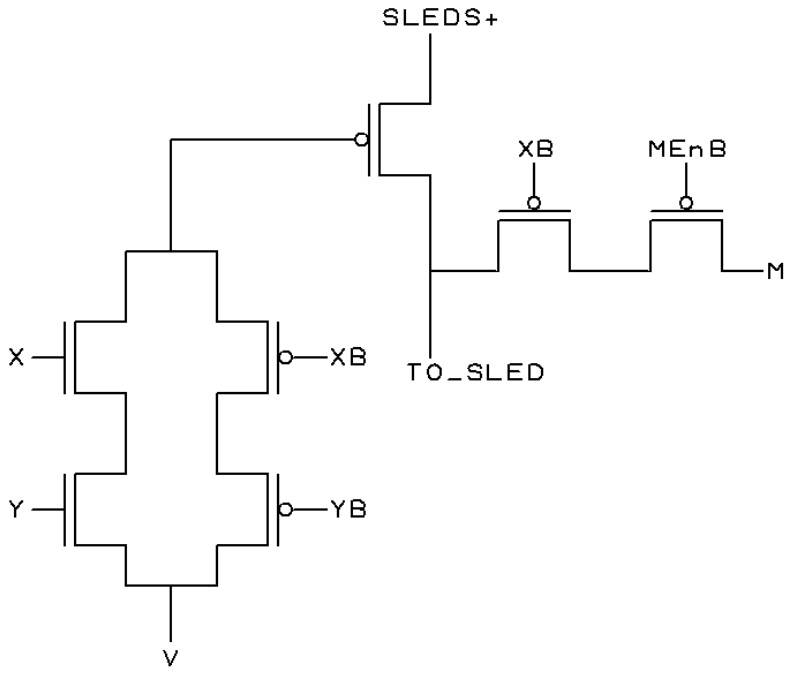


Figure 2.3: 512x512 single-color single pixel schematic

Another addition to the pixel design was the use of an analog output voltage-monitoring pin as shown to be connected to the output of the pixel by two PMOS

transistors. This allows for monitoring of the SLEDS voltage when the pixel is powered on. Two PMOS transistors were used instead of a CMOS pair in order to save space and because there wasn't a need to monitor the lower voltages.

The driver for the 512x512 pixel array was designed using ON Semiconductor's C5N 0.5 micron high-voltage CMOS technology[3]. Unlike the previous design, this was a 0.5μm process with three layers of metal, two poly-silicon layers, 12V and 20V high-voltage transistors, and a high-resistance poly-silicon.

A large constraint was that the pixel for the 512x512 array needed to fit within a 48μm device pitch. In order to achieve this, multi-fingering of the power transistors was used, which means the PMOS transistors were grouped together and shared a common N-well. As mentioned previous, the pixel also features only three layers of metal. The top layer is used to create a grid for connecting all the cathodes, while left in between are individual islands of top metal for the anode. They are not connected together. The middle layer is used for vertical connections and the bottom layer is used for horizontal connections, as shown in figure 2.4.

Due to the size of the array, another new technique had to be introduced, reticle stitching. Since the 512x512 SLEDS array, including the decoders, is too large for a single die, stitching was used to break the layout up into four 256x256 parts and then placed in a way that they all line up to reform the original 512x512 array[4]. As shown in figure 2.5, the 512x512 array is split into four sections with driver and core sections. The southeast, northwest, and northeast parts are all mirrored and rotated copies of the southwest 256x256, so this way metal paths will be aligned and they can be stitched together, resulting in our original design.

2.2 2-Color Design

As documented by Corey Lange, there is some previous work involving the 2-Color SLEDS design. An original schematic was chosen after a trade-space analysis was performed to figure out which schematic would benefit the design best. There is more detail about that analysis in chapter 3. After the schematic was chosen, a single pixel

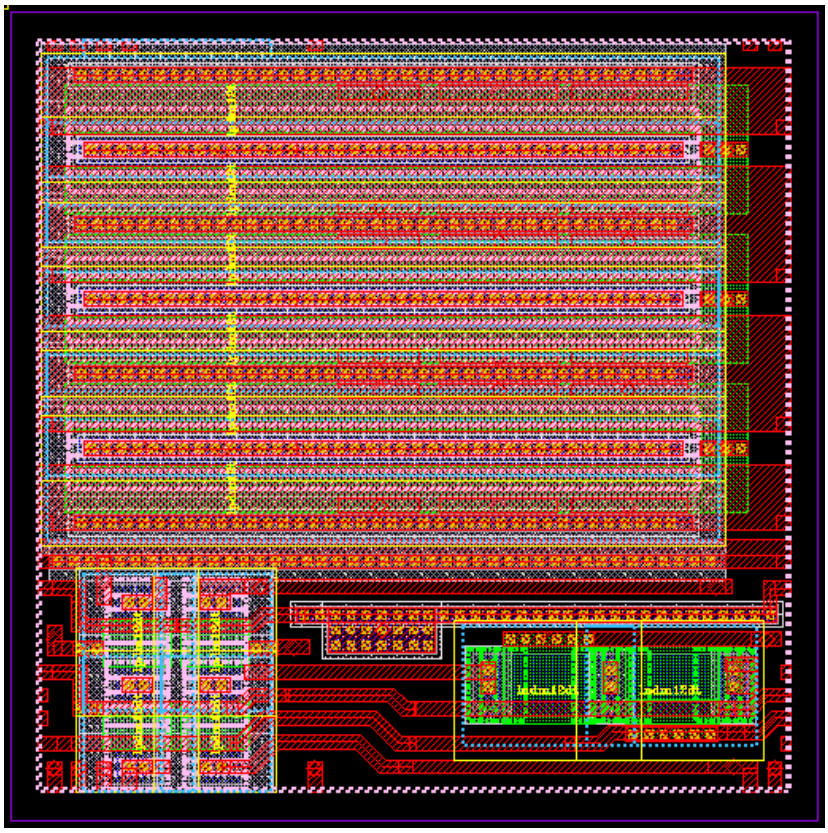


Figure 2.4: 512x512 single-color single pixel layout

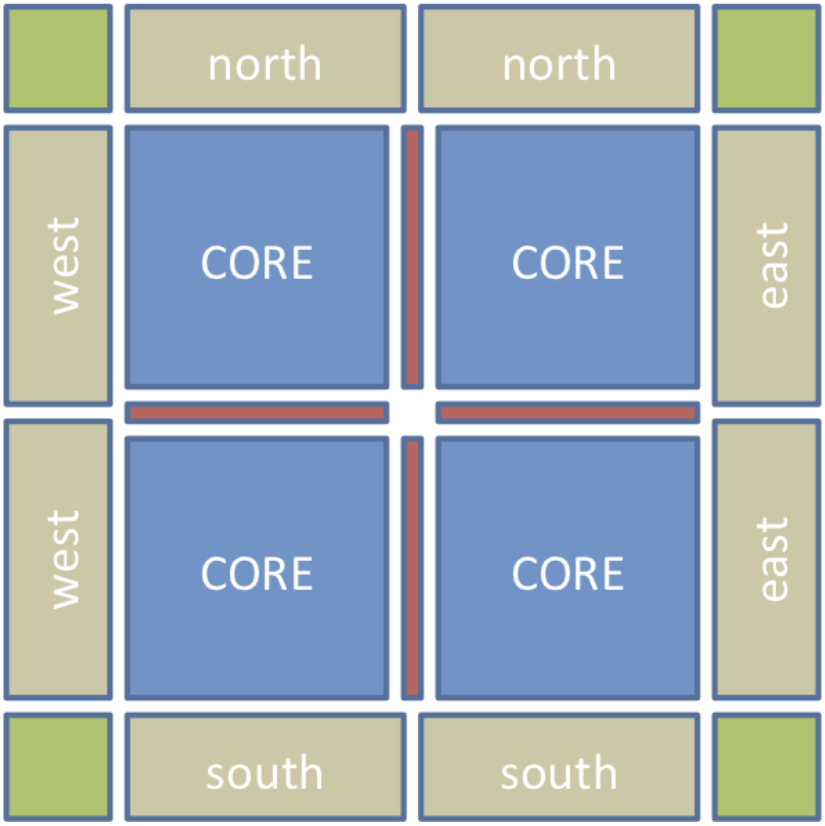


Figure 2.5: 512x512 stitching outline

layout was created, but due to ON Semiconductor's standard C5N library, the layout was unable to meet the required 48μm device pitch, since some of the standard cells were too large. To fix this problem, experimental high voltage transistors were created to reduce the size of the previous transistors. Two of these transistors are shown in the bottom right of figure 2.6. This pixel design, along with different transistor models, were sent out for testing in January 2011 so that they could be tested and possibly included in the final 2-color SLEDS design.

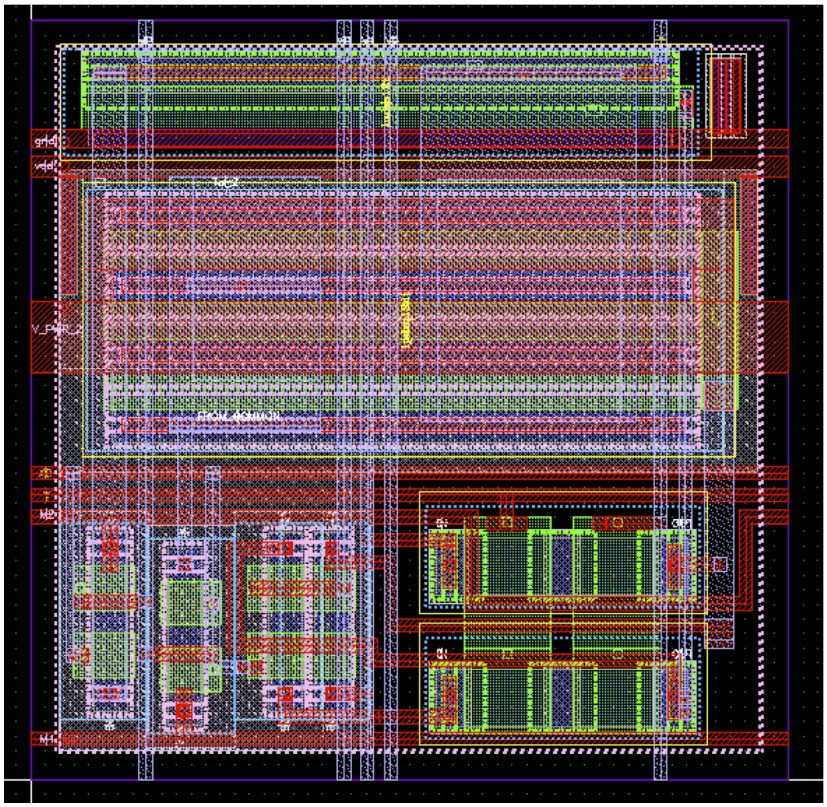


Figure 2.6: Previous proposed 2-color pixel layout

Chapter 3

CIRCUIT DESIGN

By looking at previous pixel designs, we are able to begin planning and creating a design for the 2-color pixel. Similar to the single-color design, the 512x512 2-color SLEDS array drivers use ON Semiconductor's C5N 0.5 micron high-voltage CMOS technology[3]. There were no outstanding issues with the previous design, so there was no need to change it.

3.1 Circuit Design

The design for the pixel includes a driver and pads for the LED to be bonded to. Through the driver, we are able to power and select the proper pixel out of the 512x512 array. All previous designs only featured one color to control, but this design features a 2-color design, and each LED is able be controlled independent of color or position. The key for controlling colors separately is having two separate V lines. The V pads are analog inputs (0V to 12V) that drive the SLED. Our design features two V pads, one for the first LED and one for the second. Therefore, we are able to drive the different wavelength SLEDS independently.

The current schematic started off as four separate designs, and as mentioned before, a trade-space analysis was performed to determine which schematic would work best with the SLEDS project specifications. The analysis is shown in table 3.1, and at first we were going to choose the N-type parallel structure, but we ended up deciding to use the P-type parallel structure because it uses a big NMOS, and for its better transconductance.

Table 3.1: 2-Color pixel trade-space analysis

	N-type	P-type
Series Connected	High Swing Needed Less Current Draw Difficult Independent Control More Complex Design	High Swing Needed Less Current Draw Difficult Independent Control More Complex Design
Parallel Connected	Easier Independent Control More Current Draw Needs Big PMOS Worse Transconductance	Easier Independent Control More Current Draw Needs Big NMOS Better Transconductance

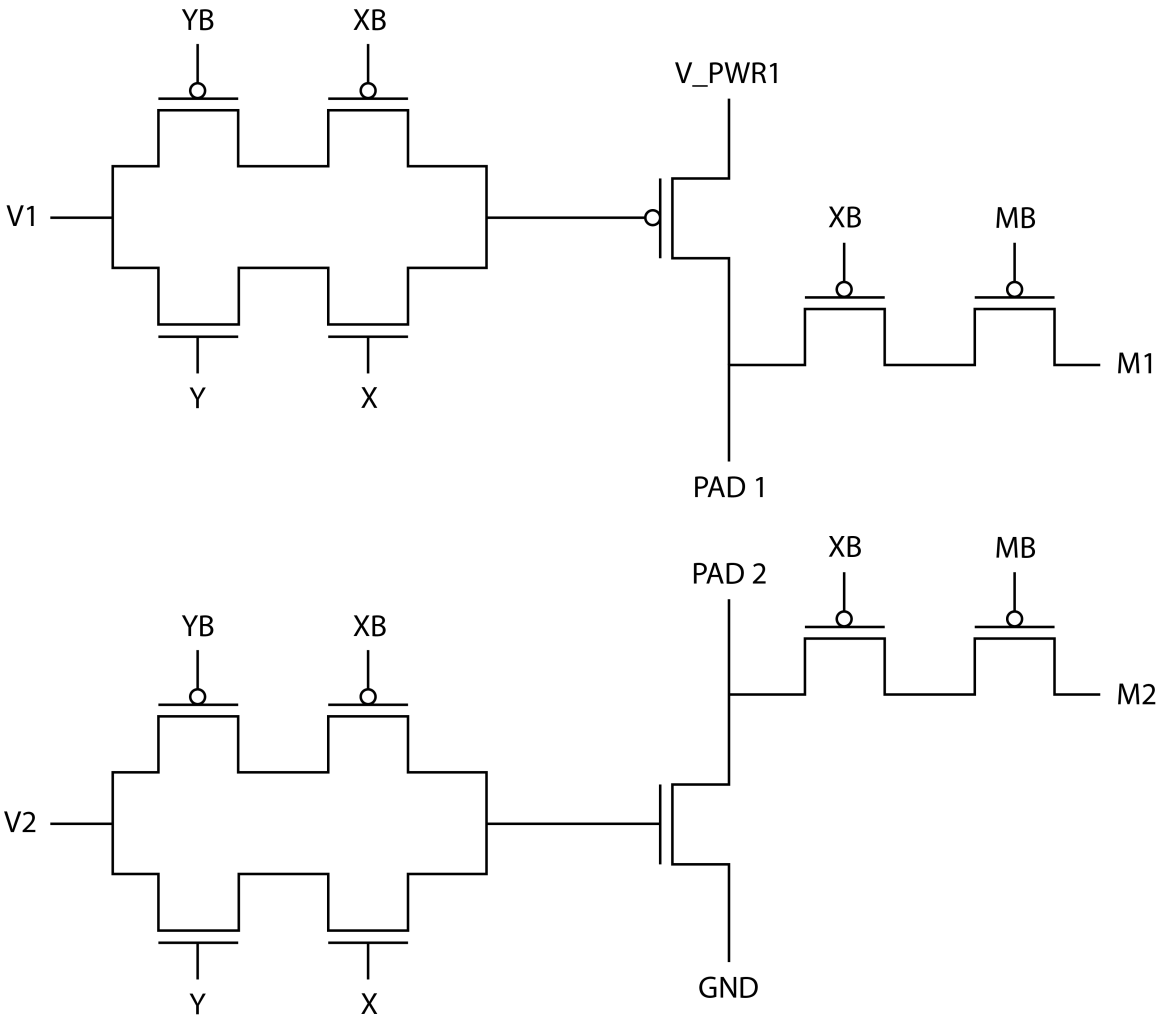


Figure 3.1: 2-Color unit cell schematic

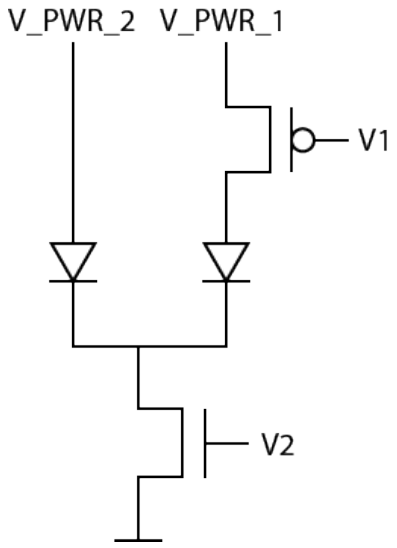


Figure 3.2: 2-Color unit cell overview schematic

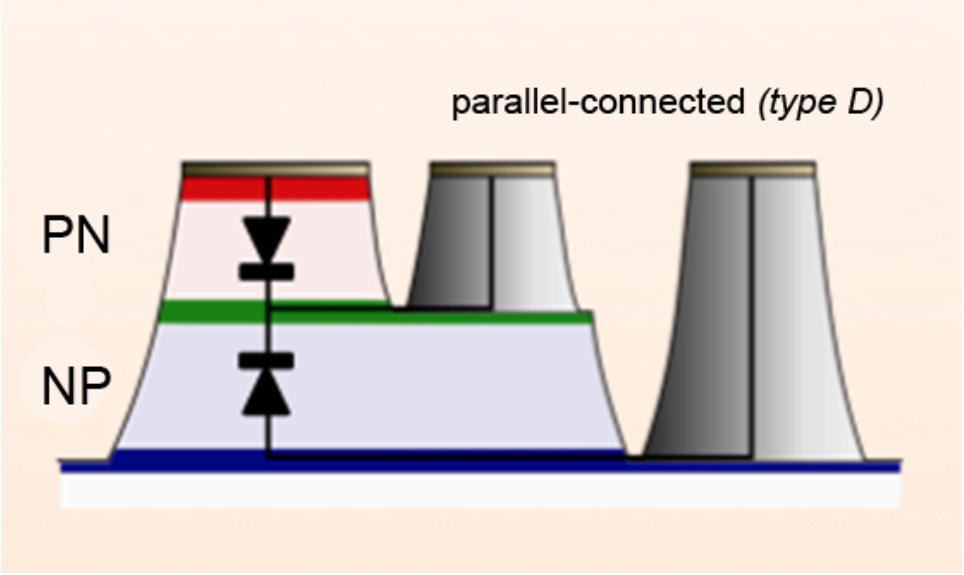


Figure 3.3: PNP SLED configuration

Another key feature of the driver design is the use of control pins to fully turn on certain pixels, and fully turn off the others. The strategy for this is the same one used in the previous single-color design, CMOS pairing. A CMOS pair is when two PMOS or two NMOS transistors are connected drain to source in order to control current flow with two gates.

Two lpdm12dt thick gate double-sided nested drain PMOS transistors are connected so that only a full 12V can pass when both gates receive 0V. These gate signals come from the lines XB and YB, which determine the drivers that should be powered in order to turn on a pixel. If only XB is low, while YB is high, the pixel will not be turned on, since only one transistor will be passing current, but the other will not allow the flow. Both rails need to be low at the same time to open up both PMOS transistors and allow 12V to flow through. At the same time, the opposite signal is at the gates of two lndm12dt thick gate double-sided nested drain NMOS transistors connected together. Due to the high signal, the NMOS transistors open up to allow the same 12V to pass. The signal lines that go to the NMOS gates are X and Y. X and Y are always the opposite of XB and YB, so if the PMOS transistor attached to the XB line is open, so should the NMOS transistor connected to the X line.

The PMOS transistors are 3.3μm wide and 2.5μm long, which is the minimum acceptable length[5]. The NMOS transistors are 4μm wide and 4.5μm long, which is the minimum acceptable length. The benefit of having the NMOS transistor in parallel with the PMOS transistors is so that the resistance can be reduced, but more importantly to take advantage of the characteristics specific to each transistor. PMOS transistors are better at passing high voltage, while NMOS transistors are better at passing low voltages. By using them both, a full 12V or 0V can be passed.

Moving through the 2-color pixel design, we next hit the transistors that are used to produce the necessary current to drive the pixel. Unlike the previous transistors, they are 12V thick gate single-sided nested drain transistors. Because the transistor needs to drive a lot of current, these transistors are much larger than the other transistors in the circuit. As explained earlier, multi-fingering is used to reduce the size of the transistors

in one direction, at the cost of expanding the transistors in the perpendicular direction. The transistor will still operate the same, but this way the transistors are able to fit into areas more reasonably.

As the driver circuit in Figure 3.2 shows, a PNP design was used for the pixel. In this strategy, the large 12V NMOS transistor handles all the current. The NMOS was chosen over an NPN PMOS current-handling design because an NMOS transistor can handle more current at a smaller size. A PMOS transistor would need to be about double the size of the NMOS transistor we are using in order to carry the same current. With a smaller full-current carrying transistor, we are able to still fit within the 48μm device pitch.

The lndm12t 12V NMOS transistor has a width of 30μm and a length of 2.5μ. Testing was conducted by Joshua Marks to ensure that a reduced 12V NMOS transistor still operated correctly at its minimum acceptable length of 2.5μm[6]. Though this transistor is smaller than the large PMOS transistor, shown in figure 3.1, it is able to handle enough current for both pixels. The location of this transistor is at the bottom of the circuit and is used to pull current in order to turn on either SLED.

The lpdm12t 12V PMOS transistor is used for providing current to the higher wavelength infrared LED. The transistor has a width of 60μm and a length of 2.5μm. Once again, the minimum acceptable transistor length was tested by Joshua Marks to insure that it would operate as expected.

Lastly, as we move across the schematic, the monitor line is left. Similarly to the previous single-color design, a monitor pin is included so that the SLEDs voltage can be measured for the selected pixel. Since this design features two colors, two separate monitoring pins are made available to measure the SLEDS voltage on either pixel, independently.

3.2 Simulation

In order to assure that our pixel design worked correctly, we ran simulations on the schematic. To do this, we first created a test bench environment so that we

could control what values were being passed into the pixel, shown in figure 3.4. For this simulation, we are checking to see how much current is drawn by the two colors and what voltages are needed to turn each pixel off. For this set up, X and Y are set to high (12V) in order to turn on the NMOS transistors and XB and YB are set to low (0V) to turn on the PMOS transistors, allowing the V1 and V2 signals through. V1 and V2 are set in the analog environment, making it easy to change them when simulating, but for now, V1 is set to 0V in order to turn on the large PMOS and drive current to the high wavelength SLED, while V2 is set to 12V in order to turn on the large NMOS transistor and drive current to the low wavelength SLED. V1 will be used for sweeping to help determine the voltages necessary to turn off the LEDs.

V_PWR1 and V_PWR2 are also controlled within the analog environment. The reason for this is so that these values can be changed around to figure out what voltages are necessary to turn each LED off. Simulation results are show in figure 3.5. For that simulation, a DC voltage sweep was used to check the change in current for both LEDs. The sweep was on V1 from 12V to 0V with 1000 steps, which should first turn the low wavelength LED on because the high voltage will turn the large PMOS off, and as V1 decreases, the large PMOS transistor will slowly turn on resulting in the high wavelength LED turning on and the low wavelength LED turning off.

3.3 VLSI Layout

As mentioned before, the same technology used in single-color, ON Semiconductor's C5N 0.5 micron high-voltage CMOS technology, was used again, and the pixel needed to fit in the same devise pitch, 48μm. Due to the size of the pixel, it was physically impossible to fit a PMOS transistor as big as the previous design within the space provided and still pass Design Rule Check (DRC). Because of this, both the large PMOS and NMOS were scaled down to 75% of their previous widths. By scaling the two transistors equally, we were able to maintain the same current ratio, and with a 25% reduction, there was just enough space to fit the rest of the circuit without causing any errors.

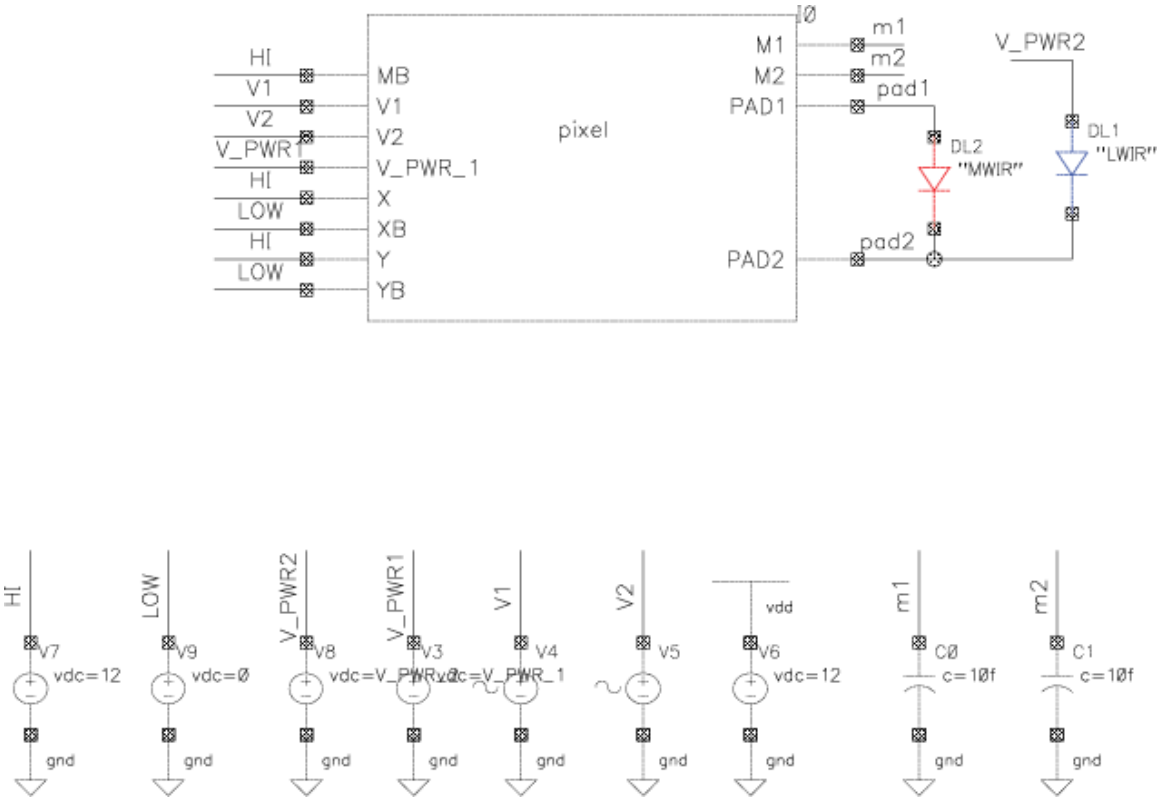


Figure 3.4: Pixel test bench

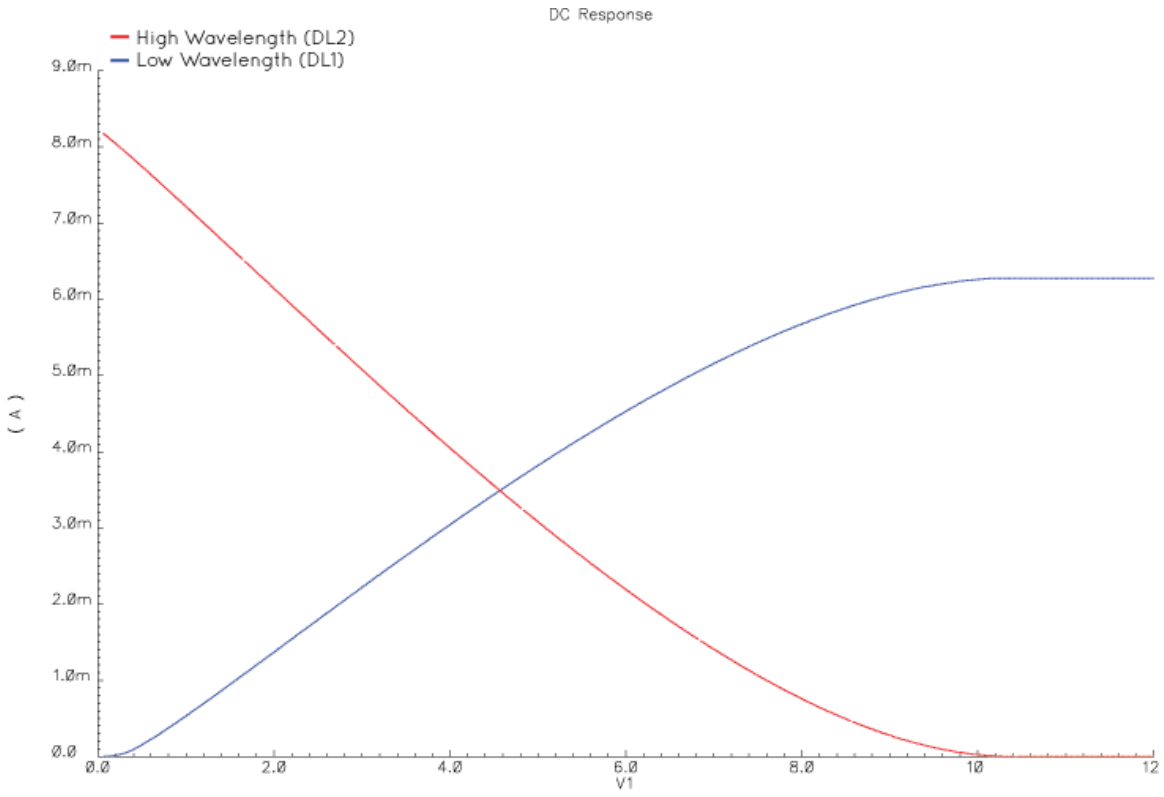
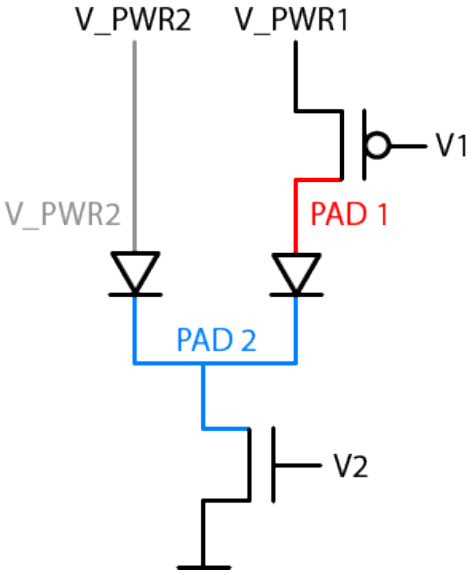
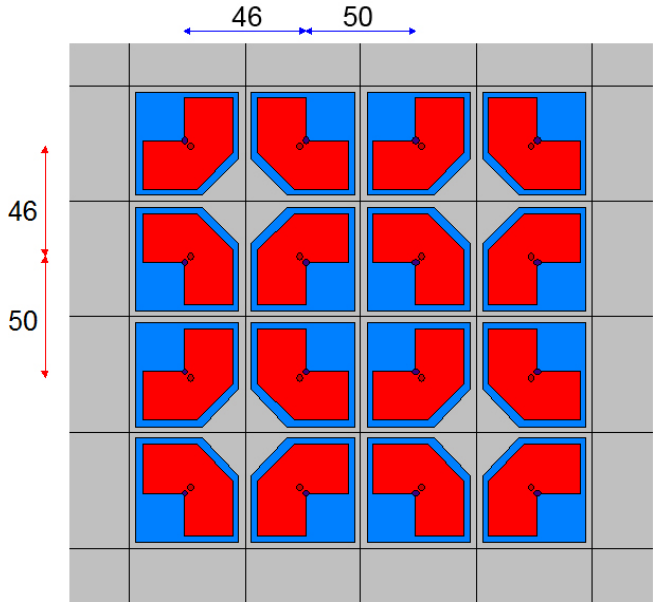


Figure 3.5: Pixel test bench results

In our design, three metal layers are used. The top metal layer is used for device contacts. There are three glass cuts in order to touch down on these areas. As shown in figure 3.6, the top metal mesh array is used to distribute V_PWR2 throughout the array, and the other two pads are for local connections to the circuit. Pad 1 is used as the anode contact for the higher wavelength LED, while V_PWR2 is used as the anode contact for the lower wavelength LED. Both infrared LEDs have their cathodes connected at Pad 2.



(a) Overview schematic with pads highlighted



(b) Top layer metal layout with pads highlighted

Figure 3.6: Match up of schematic to layout pad locations

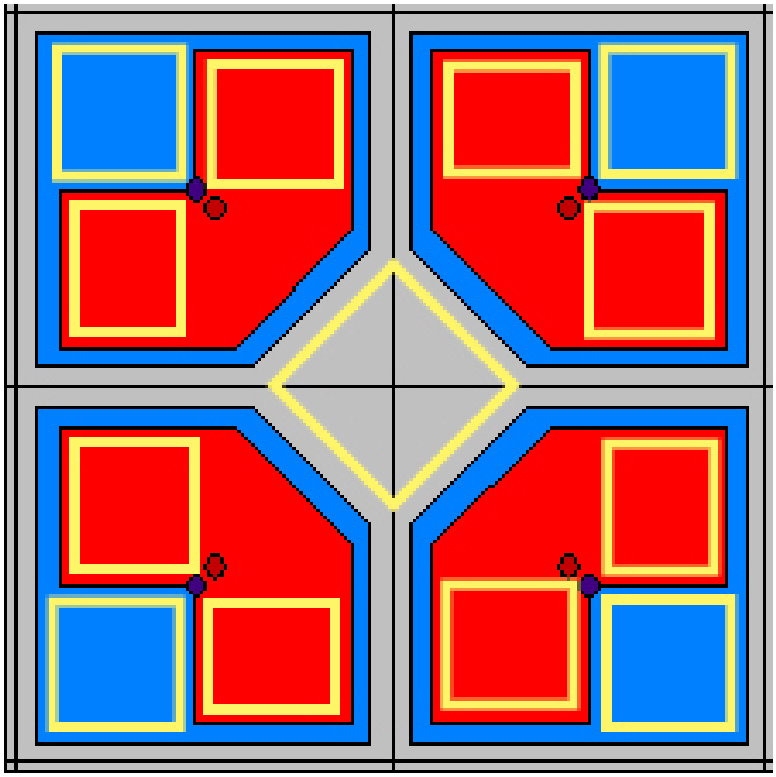


Figure 3.7: 2-Color single pixel glass cuts

The other two layers of metal are used for routing within the layout. For the most part, the bottom layer is used for horizontal routing, while the middle layer is used for vertical routing. Since tiling is necessary for this layout, due to the size, the rails must line up from one quarter to the other. Vertical rails are made with the middle metal layer, and horizontal layers are made using the bottom metal layer. Vertical rails must be able to line up, vertically, from one end to the other, so that when two quarters are placed next to each, the rail will continue. This must also happen with the horizontal rails, but the lines must line up horizontally at both ends.

As mentioned before, we needed to tweak transistors to their minimum acceptable lengths in order to assure we would have enough room to fit the pixel layout within a 48μm device pitch. Besides reducing the larger NMOS, larger PMOS, and smaller PMOS lengths to 2.5μm and the smaller NMOS lengths to 4.5μm, we also adjusted the ON Semiconductor's standard C5N library standard cell layouts for both smaller sets

of transistors. Since we would be using two PMOS transistors or two NMOS transistors in series, it made sense to reduce size and metal use by connecting the source and drain of a pair together at the substrate level. This way, we would be able to have our transistors connected and not have to worry about losing space to route metal, since the connection would need to be at the bottom or middle metal layer, and that could make it difficult to run vertical or horizontal rails or interconnects. By doing this, we were able to reduce the size of the NMOS transistor pair by 0.4μm and the PMOS transistor by 1.7μm.

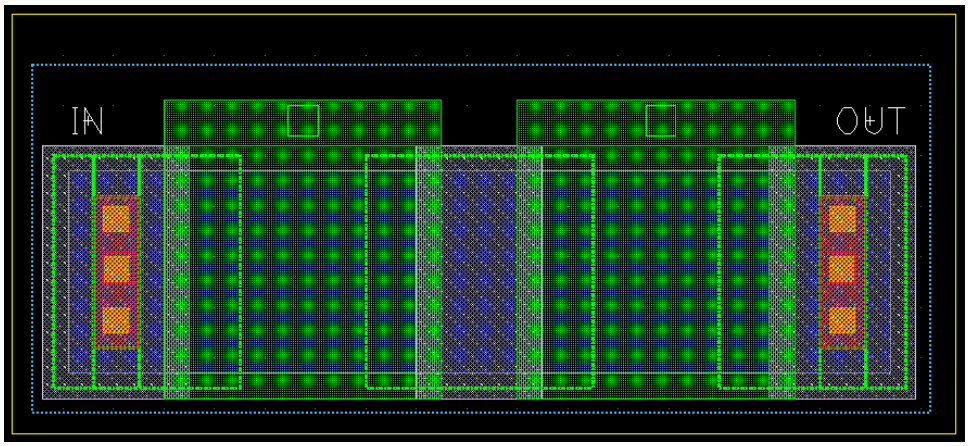


Figure 3.8: Modified NMOS transistor pair

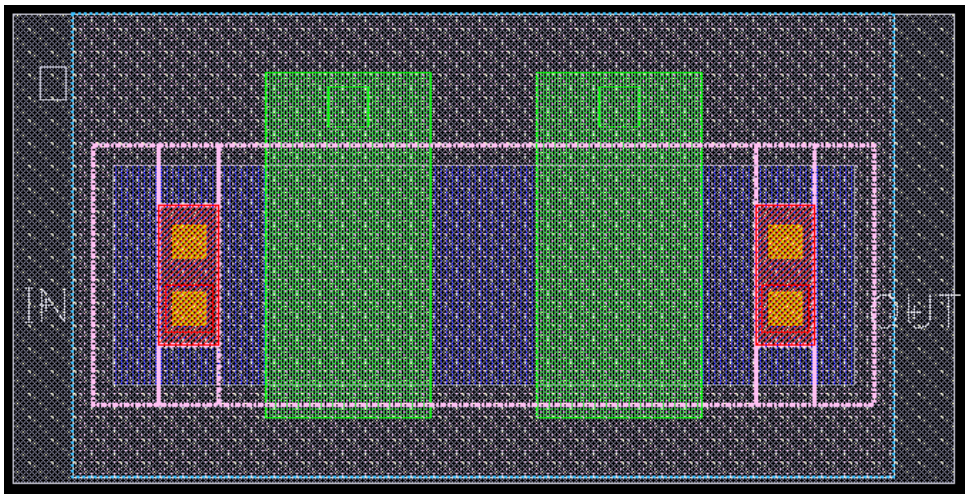


Figure 3.9: Modified PMOS transistor pair

Chapter 4

DESIGN METHODOLOGY FOR BUILDING SUPER ARRAYS

When building a super array, it is important to keep in mind how a pixel will multiply and fit together with other pixels, since it would take too long to build a 512x512 array pixel by pixel. Creating a large array takes much planning and consideration, at first, but this saves time in the long run. Rails must be able to fit together and layers must be properly spaced so that when two pixels are placed next to each other they won't cause a DRC error or short.

4.1 Design Process

The process of scaling begins slow, but speeds up rather quickly. The first thing to do is build the pixel, but there are considerations to keep in mind while building. Any metal must be far enough from the outsides so that when mirrored or tiled, another pixel won't have the same layer close enough to cause an error. The spacing distance between tub layers is 4μm, so when placing transistors, it is important to think about how a mirrored pixel next to the current one will look, and adjust the transistor far enough from the outside that there will not be a problem. Normally, this means spacing that transistor more than 2μm from the edge, since if there is a mirrored layout next to this, that distance will double and therefore be acceptable. If a pixel is being rotated, it is important to think about how another side will line up to the current pixel's side.

It is necessary to think about how rails and routing will flow. Rails must be able to run continuous from one pixel to another, which means one pixel's rail end must match up to the other. You also don't want routing lines to short to another pixel, spacing them far enough from the edge, or in an area that won't be overlapped is something to keep in mind.

Once the pixel design is completed and passes DRC and LVS, the next step is to create a 2x2 array. This way, we can see how the pixel interacts with surrounding pixels. As mentioned a couple times previously, you don't want layers to connect or be too close if they're not supposed to be, and even if the single unit passes DRC and LVS checks, that doesn't mean it won't cause errors once other pixels are around.

First, a 2x2 schematic must be created. As shown in figure 4.1, this super pixel, as it is often referred to as, is wired up the same way a 512x512 pixel would be. Vertical rails are connected together for each column, horizontal rails are connected together for each row, and anything else that needs to be connected or kept separate is done. Not only will this help us make sure nothing is shorted in the LVS check, it will give an earlier warning of displaying error markers if pixels have layers that overlap incorrectly.

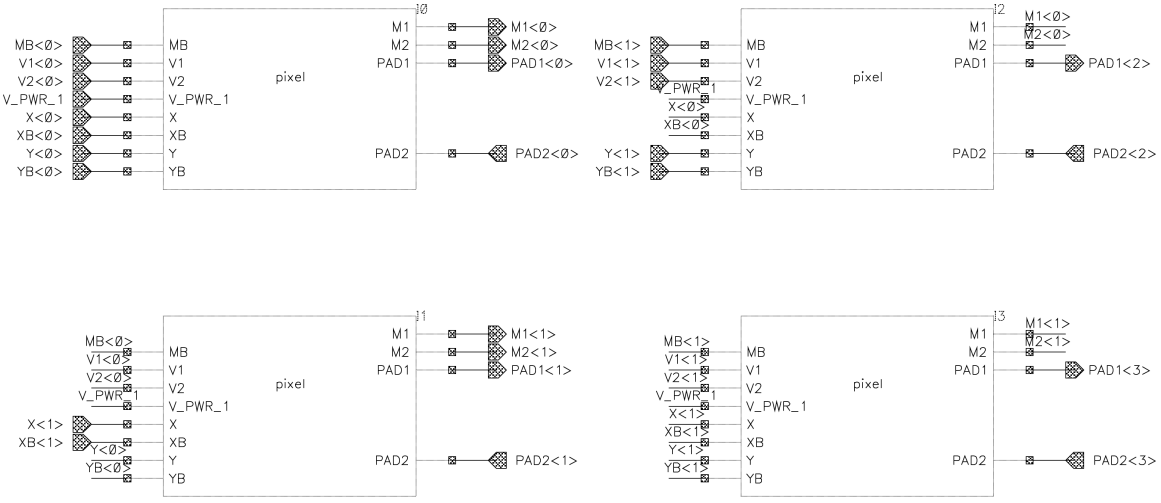


Figure 4.1: 2-Color 2x2 array schematic

A test bench is also created to assure that this super pixel is functioning correctly. In the setup, we are using the same decoders as the single-color 512x512 design, but two additional pins have been added for the second analog input and monitor connections. The decoders combined with the 2x2 SLEDS array are meant to simulate the southwest quadrant of the chip, since the chip needs to be broken up into fourths when getting fabricated. The test bench schematic is shown in figure 4.3, and the results are shown in figure 4.4.

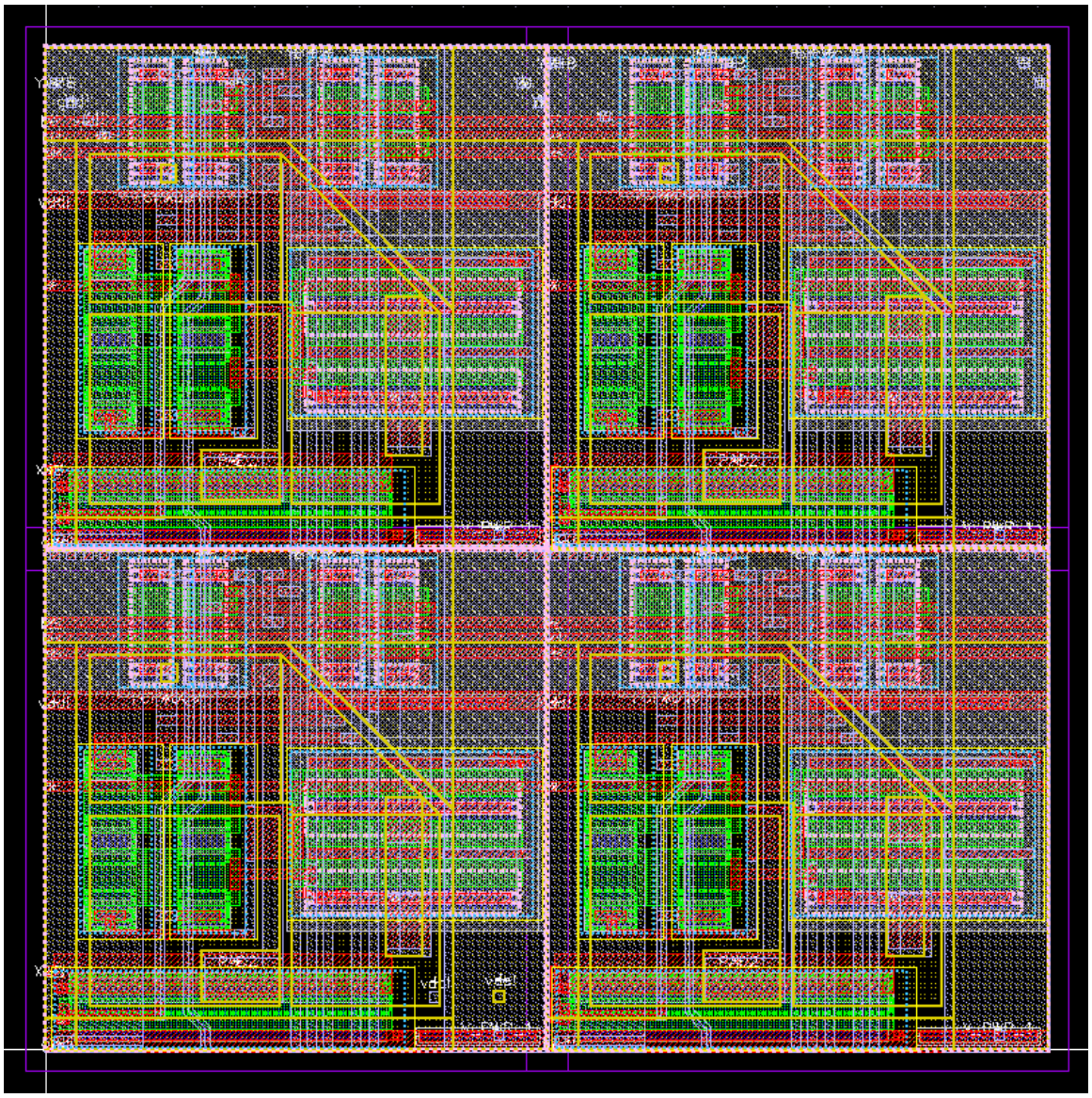


Figure 4.2: 2-Color 2x2 array layout

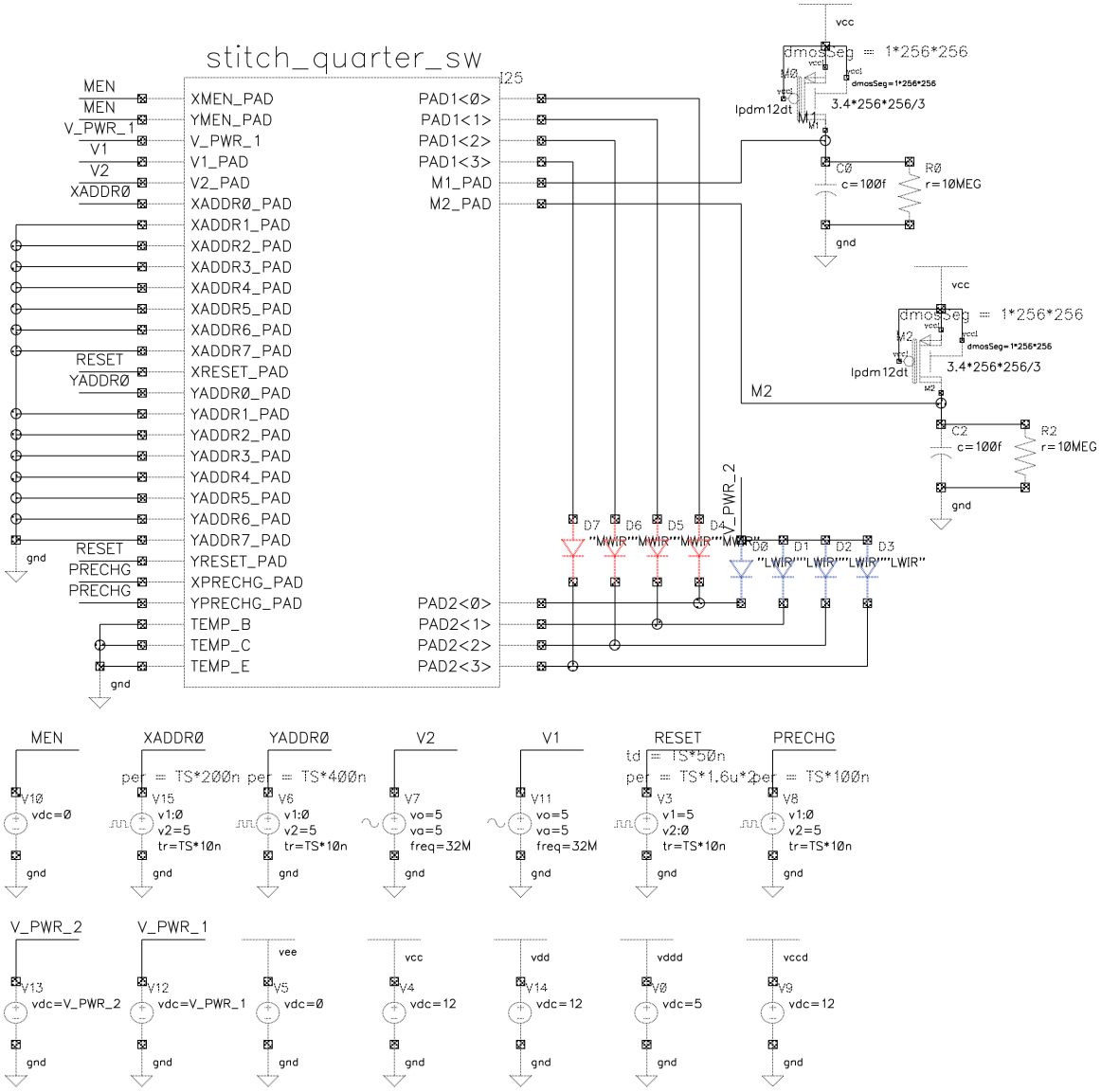


Figure 4.3: 2-Color 2x2 array test bench

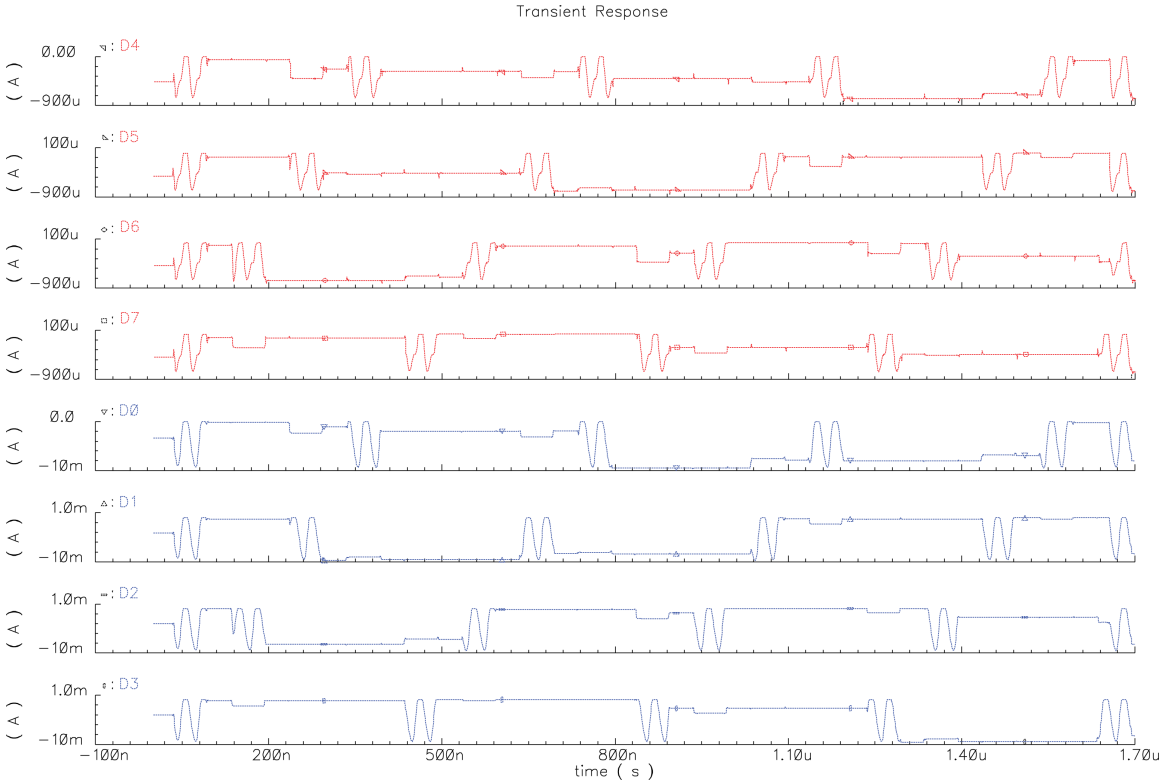


Figure 4.4: 2-Color 2x2 array simulation results

4.2 Scaling from 2x2 to 512x512

The layout for the 2x2 southwest design needed to be complete, first. This includes the super pixel and decoders. Some of the parts from the previous SLEDS chip can be used again, as mentioned before. The parts might need some adjusting, though, in order to match up with our new pixel design.

For the 2-color design, the pixels are tiled differently than the single color 512x512 SLEDS array. The single-color array could be scaled without any change to the pixel orientation, since all the contacts were handled on a single pixel, but this is not possible for our new 2-color design. Since there is a shared power line (V_PWR2), the V_PWR2 pad area must match up with the same pad area of the other pixels within the super pixel, as shown before in figure 3.7. Because of this, there needs to be two different types of connections between the decoders and pixels for each side of the pixels. Horizontal and vertical decoders must be able to connect to the pixel in normal position as well as when it is mirrored. The two types of connections are shown in figures 4.5 and 4.6.

The pad layout for the 2-color array must also be changed so that we have pad connections for the two power lines, V_PWR1 and V_PWR2, and ground. The top metal that was previously used to feed VCC and VEE to the SLEDS array has now been split into three lines. The largest line is for ground, since it must be able to handle all the current flowing down through the SLEDS, and this could be around 20mA (10mA from each diode), so the metal path is 22.2μm wide. The other two paths that carry V_PWR1 and V_PWR2 must be able to handle around 10mA each, so they are both sized at 11.1μm each. These pad paths run both horizontally and vertically, which helps to reduce the current on any side of the array.

Creating the 2x2 southwest design provides a great opportunity to make sure the different parts of the array not only match up correctly, but also helps to reduce any chance of DRC or LVS errors at the top level. DRC can be run on the 2x2 southwest pixel without any problems. Unfortunately, pads create a problem with running LVS, so before running LVS on the layout, the pads should be removed.

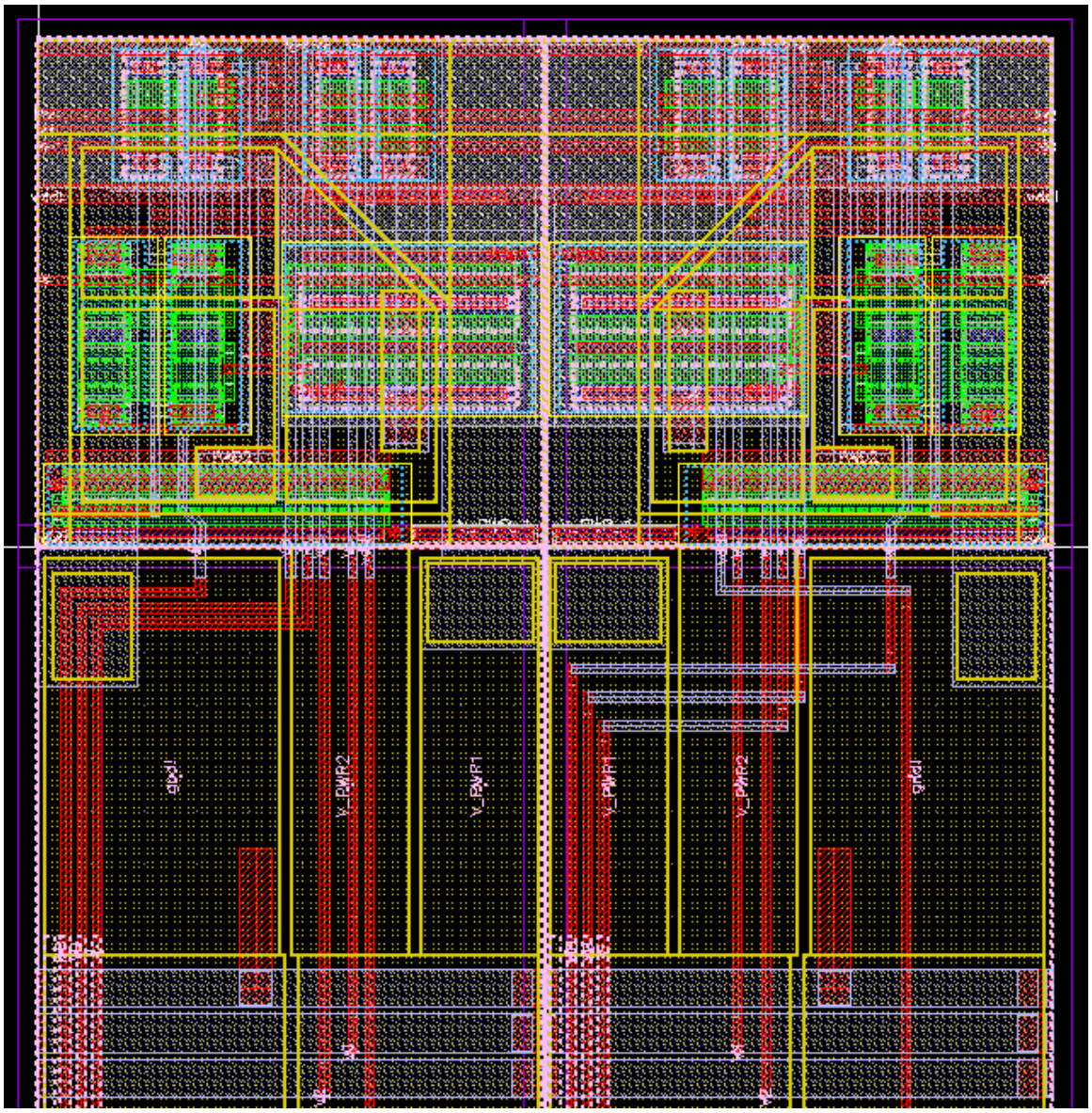


Figure 4.5: South adapters to connect the drivers to the array

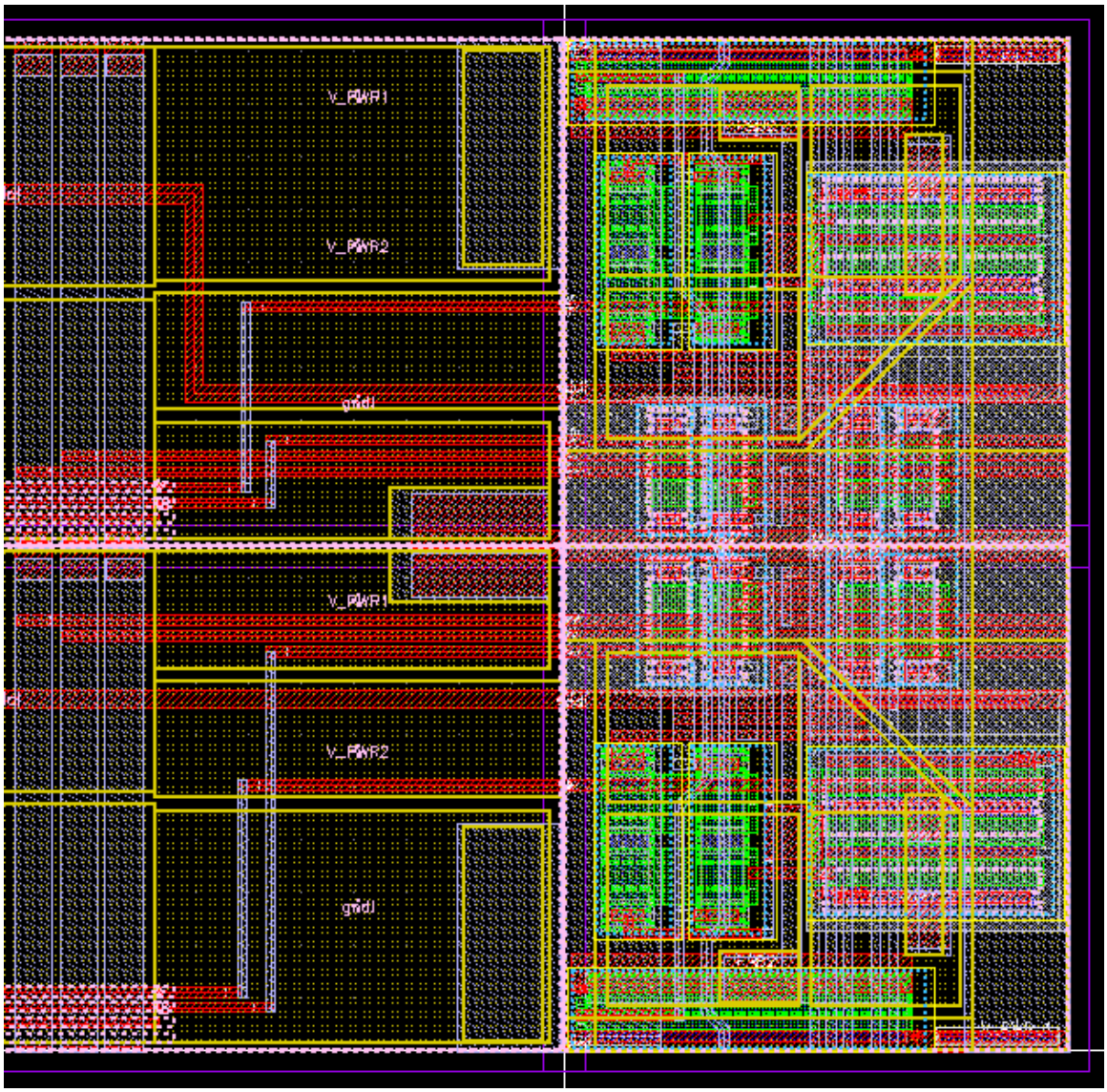


Figure 4.6: West adapters to connect the drivers to the array

Once the southwest 2x2 SLEDS array passes DRC and LVS, the next step is to design the 512x512 array layout, since the larger array is made up of pieces from the smaller array. As mentioned previously, this design will only be for a 256x256 SLEDS array, since stitching allows us to combine four 256x265 arrays to create a 512x512 SLEDS array.

The first step then is to create the 256x256 array of pixels. Previously, the designer could instance 256 pixels horizontally and vertically, but since the two-color design uses mirrored and rotated pixels, the 2x2 super pixel is instanced instead to create a 128x128 array of super pixels, which is a 256x256 array of SLEDS pixels. Figure 4.7 shows how the separate super pixels line up within the large array.

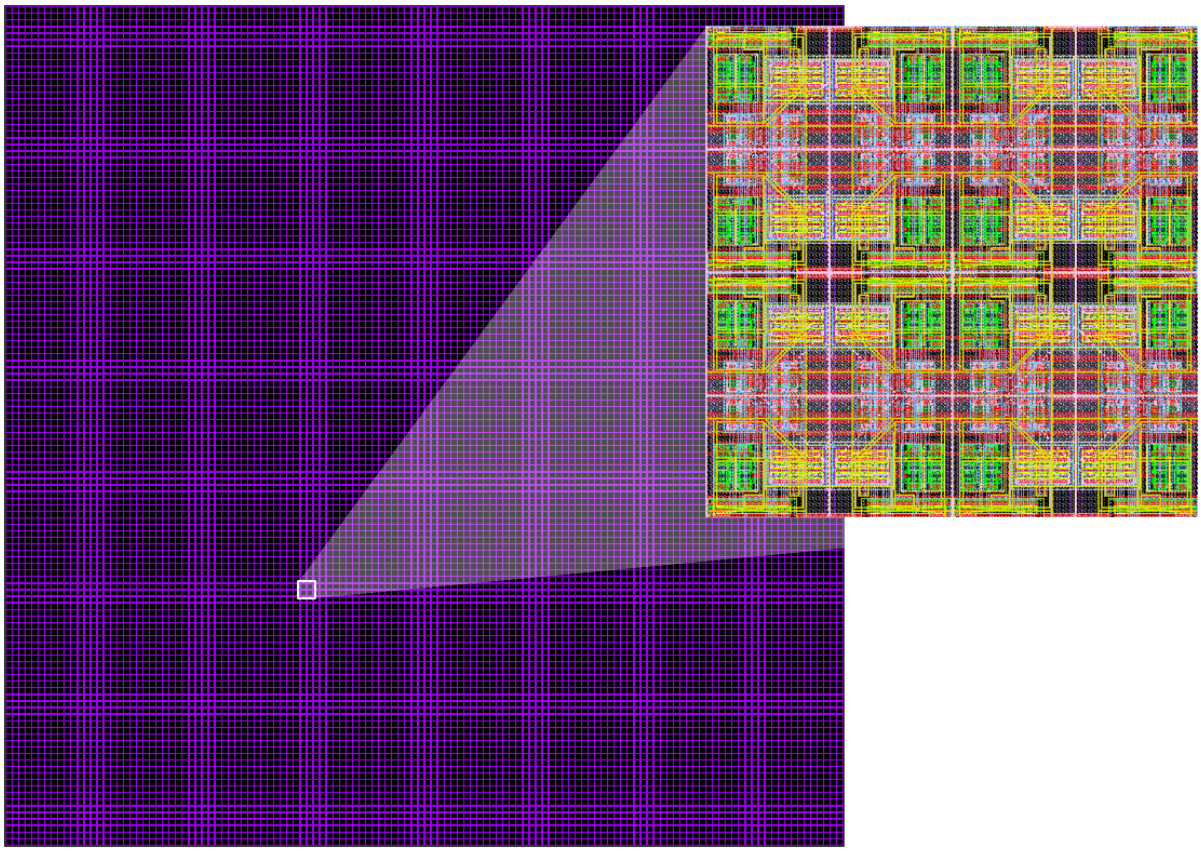


Figure 4.7: 256x256 SLEDS array with 2x2 super pixel sample expanded

With the core array created, the next step is to instance the south and west decoders. Similar to the pixel array, the decoders are no longer instanced as an array of 256 in one direction. Due to every other pixel being mirrored, the decoders must also be changed to connect correctly to the pixels and therefore are grouped together with a decoder that fits on pixel and another that is designed for the same pixel but mirrored. 128 of these decoder pairs can then be instanced in one direction to result in 256 decoders that connect properly to each pixel in the core array.

To provide power to the pixel and drivers, pads are lined on the two of the sides of the quarter (when stitched together, pads will line the four sides) for the three main rails: gnd! (ground), V_PWR1, and V_PWR2. Previously, the single-color design only needed two rails, VCC (12V power supply) and VEE (0V power supply), but as mentioned before, the 2-color design requires two supply rails, V_PWR1 and V_PWR2, to power the SLEDS (one rail for each pixel), and a ground rail. 32 pads line one side of the array, and they are divided up between the three rails so that V_PWR1 gets 10 pads, V_PWR2 gets 11 pads, and ground gets 11 pads since it handles more current than the other two. In order to connect to the pads, the three rails are split up between the three metals. This allows rails carrying the same supply to become interconnected without interfering with the other rails. V_PWR2 uses the top metal to connect to the pads and to create an interconnection between rails, V_PWR1 uses the middle layer to do this, and ground uses the bottom layer.

To finish up this stitch corner, the southwest pad section should be added to the lower left-hand corner of the design for the analog input and output pads, address pads, and the power pads for the decoders. Figure 4.8 shows the completed layout for the southwest stitch quarter, which includes the southwest pads, decoders, and 256x256 SLEDS array (many details cannot be seen in this figure because it is at such a large size to see the full layout that the individual pixels are too small to render).

The southwest stitch quarter layout can be used to create the other three stitch quarters. As shown back in figure 2.5, there are also decoders on the north side and the east side. The north decoders are the same as the south decoders, but mirrored around

the horizontal axis. The east decoders are the same as the west decoders, but mirrored around the vertical axis. The southwest pads section (the square in the bottom left of figure 2.5) can be mirrored around the vertical axis to create the southeast pads section, mirrored around the horizontal axis to create the northwest pads section, and rotated 180° to create the northwest pads section.

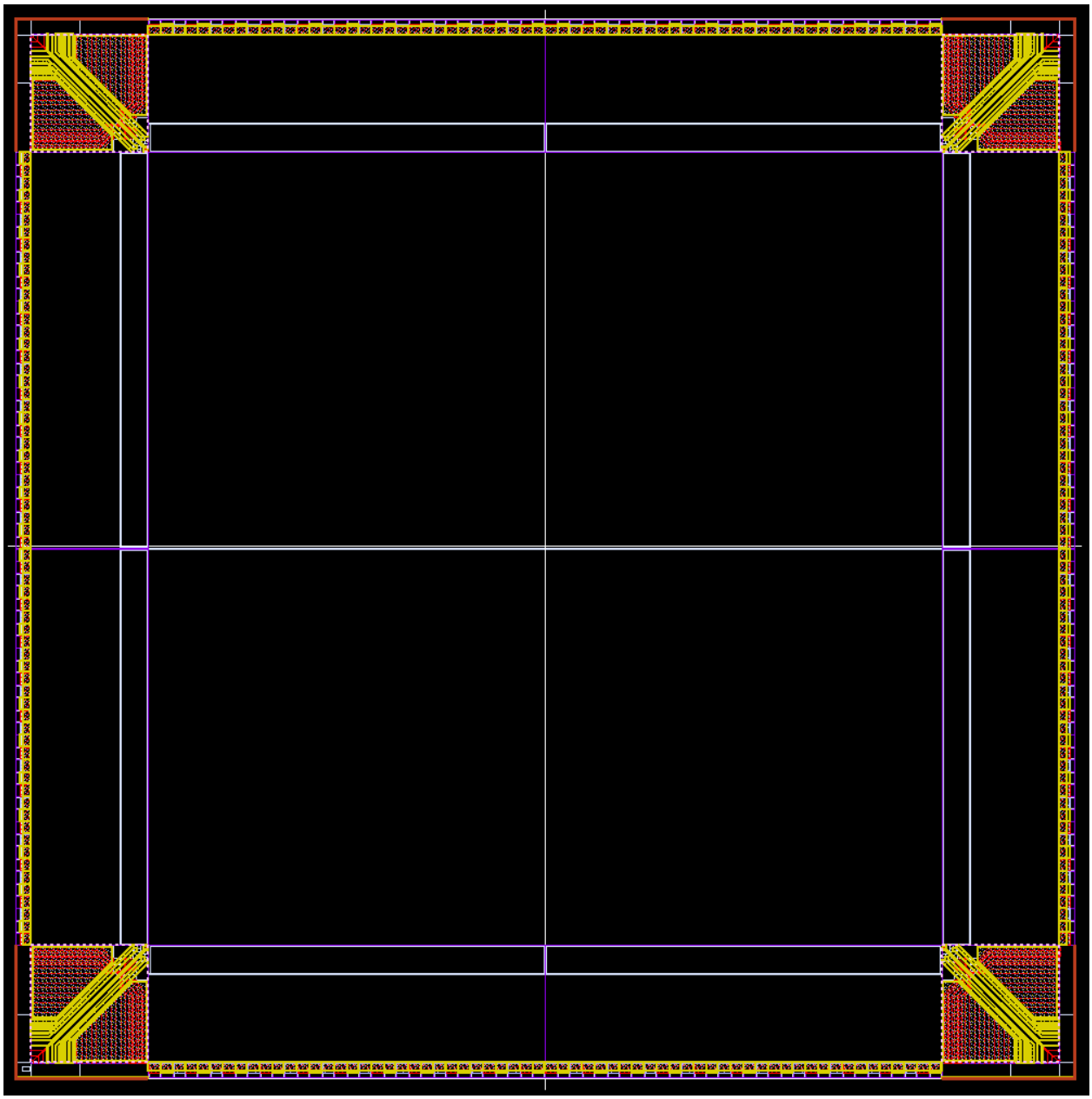


Figure 4.8: Southwest quarter layout

Chapter 5

TECHNIQUES TO IMPROVE YIELD

5.1 Examine Previous Mistakes

When I started on the SLEDS project, I began by testing the single-color 512x512 SLEDS wafers with the system Corey Lange developed to make sure everything was functioning correctly, before we sent them off to get bonded. One problem we came across more than any other was that the SLEDS+ and SLEDS- lines were sometimes shorted. This is bad because the SLEDS+ and SLEDS- are two of the main power rails throughout the system, so shorting them would cause countless problems.

To improve future yields, it is important that this issue be examined to figure out why there was consistent shorting between SLEDS+ and SLEDS-. To do this, one of the single-color wafers should be powered up using the probe station and a thermal camera can be used to observe where the short might be occurring, since that area should be heated more than other areas. Once the area of the short has been confirmed, the old layout should be reviewed to figure out how this short could have happened. Once we know why it happened, we can fix the error so that it doesn't occur again.

5.2 V Line with Transmission Gate

As the SLEDS array grows to a larger size, yield becomes a big factor, since the chance of error increases with the size of the object. An array of 128x128 pixels not only has a smaller area for an error on a wafer to occur, more of those arrays can be produced since they would be smaller than a 512x512 array. More details about improving yield with larger arrays will be discussed in the next section.

One proposal to improve yield is to make it that bad pixels or sections of the array could be turned off in order to reduce the damage incurred by a short. Transmission gates would need to be added to the analog V lines for the pixels, and the column section driver could be used to switch the V line on or off. The column selector already produces a signal and inverted signal line, so it would work perfectly with the transmission gate to either turn both the PMOS and NMOS transistors on at the same time, or off as shown in figure 5.1. If after initial testing there was a bad section of the array discovered, that area could be avoided and never powered on, since the chip could be set up to send a high value on V1 and a Low value on V2.

Due to the nature of the transmission gate, when a column is not selected, the transmission gate output will be floating. Therefore, it would be good to also add an additional transistor on the output side of both lines that would tie the V1 line to 12V in order to turn off the PMOS, and tie the V2 line to 0V in order turn off the NMOS.

Along with allowing more control over bad areas of the SLEDS, this technique provides a safety net for testing. Currently, if the SLEDS design is not constantly refreshed, leakage will slowly turn all pixels on. With the added transmission gates in place, all of the V lines will be tied to positions that power off the pixels and therefore if there is ever a problem refreshing the chip, it will not be as big of a problem, since there is no room for leakage.

5.3 Tiling

The next step in the SLEDS project will be fabrication and testing of the 2-color 512x512 SLEDS array. This will be similar to the testing of the single color 512x512 SLEDS array, but will require a new interface board, since we are using new power supply rails for the SLEDS devices, instead of the previous ones. We also have a different setup for analog inputs and outputs, since there are two of each (a set for each color), instead of the previous design which only needed one of each because it was a single color.

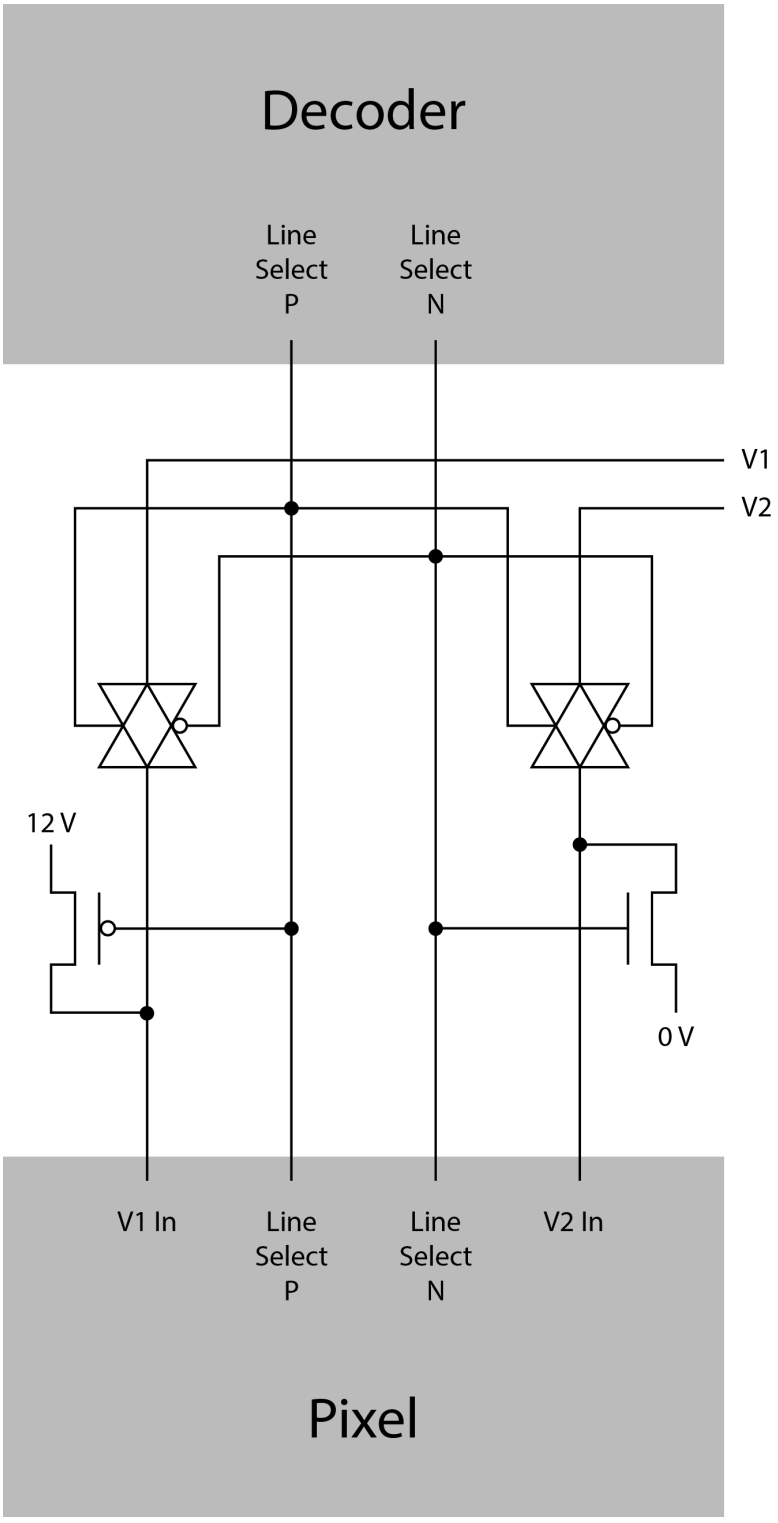


Figure 5.1: Decoder to pixel with transmission gates on V lines

The next SLEDS array design will most likely be a larger array, and this will create complications, since as the arrays grow in size, yield drops. The expected yield for a 2kx2k array is much less than 1%[7]. It is harder to fabricate larger arrays without any errors, so a new strategy will need to be used in order to improve yield, tiling. Coupled with quilt packaging (developed at Indiana Integrated Circuits), tiling can be used to connect two sections of a chip together at micron level with edge overlap that prevents gaps between array 'tiles'.

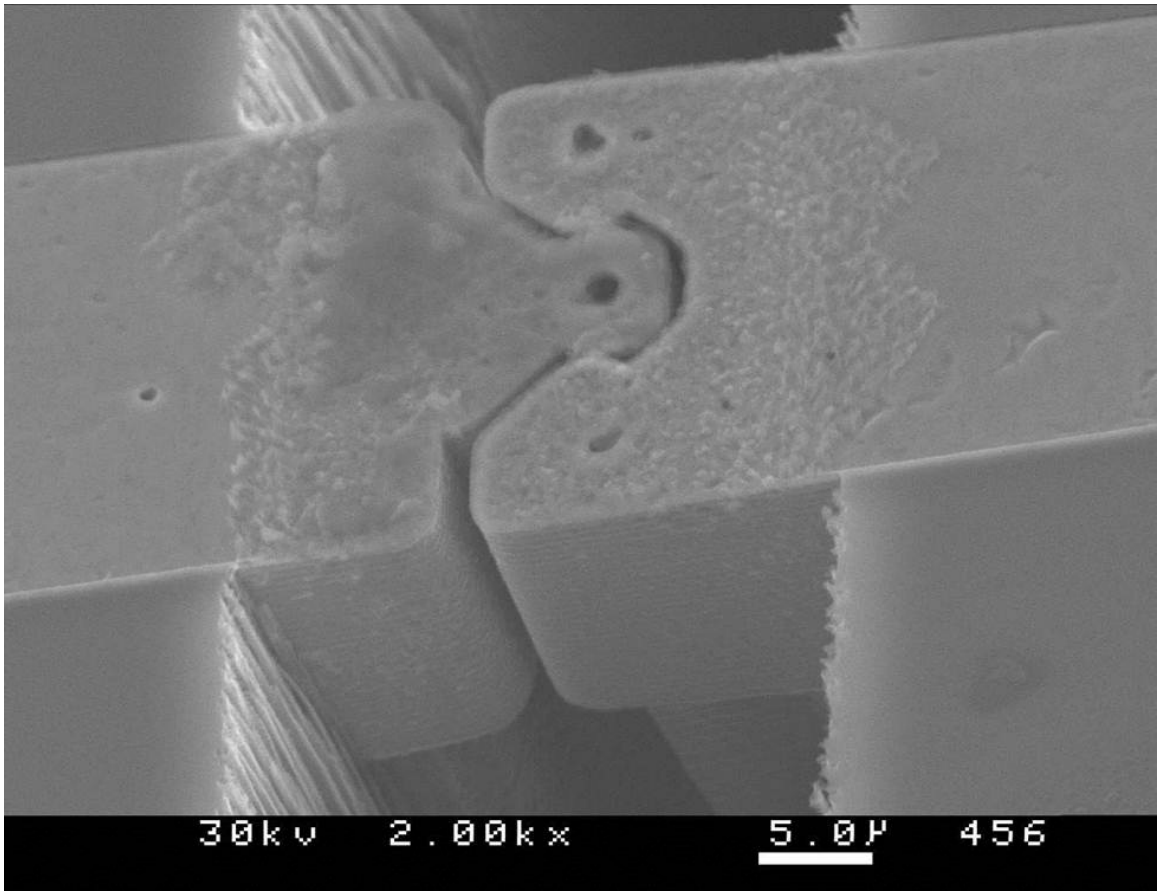


Figure 5.2: Quilt package connection

By using 512x512 as a basic block size, larger arrays can be built with different numbers of blocks, such as nine 512x512 blocks for a 2kx2k array, and 64 512x512 blocks for a 4kx4k array. With a yield average over 50% for a 512x512 die from an 8"

wafer, it would be reasonable to create larger arrays using this tiling method, and the custom emitters will only require a new carrier design when sizing changes.

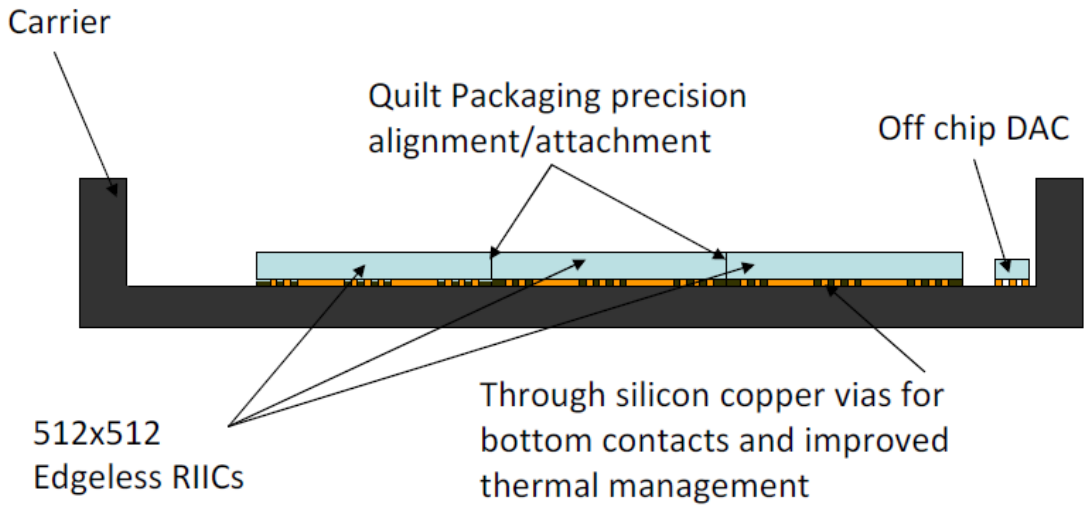


Figure 5.3: Scalable tiling outline

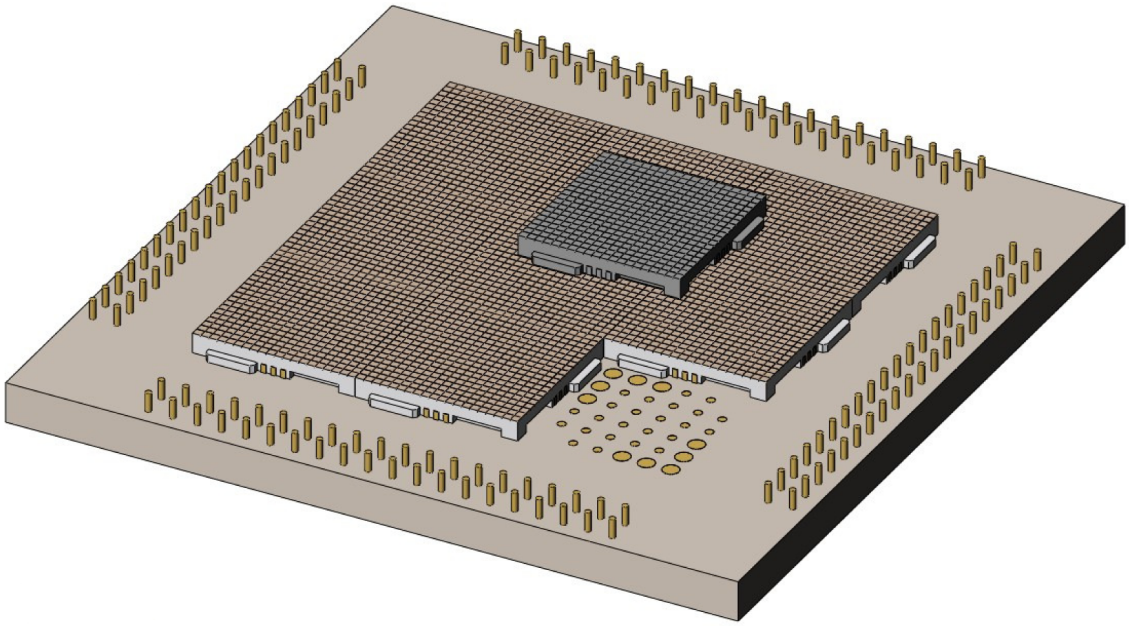


Figure 5.4: 2kx2k tiled array example with a tile removed

Chapter 6

CONCLUSIONS

Though the resolution of the design was not changed, with the additional pixel color, we are able to create a more realistic simulation environment. With an additional color, infrared signatures can become more complicated and accurate, which is better for calibrating and testing a detection system.

The single-color 512x512 SLEDS system was a great Improvement over the previous 68x68 system. It also helped to create a beginning platform for the 2-color design to move into. By keeping the same device pitch, 48μ, we are able to almost use the same decoders as before, since the new 2-color 512x512 array can replace the old single color array without changing any sizing. There were minimal changes that needed to be applied in order to connect the new array, since the previous pad routing was not the same and two new pins were added in order to send and monitor the analog signal needed for the second LED.

By using the previous decoder design, we are still able to use domino logic in order to light pixels simultaneously, and occasionally in parallel, due to the four separate quadrants and decoders. This also works with the multiple colors, since each pixel operates on a separate analog control line, so they can be independently controlled. This will be tested further once the chip is fabricated in the next step of the SLEDS project. Hopefully, due to the yield improvements, there will be a greater production of working chips to be tested.

This chip provided a great opportunity to outline the design process for a SLEDS pixel array, since it has not been discussed before. It is important to know how to approach a design as large as the SLEDS chip, and hopefully this process can continue to be used, as it has been used with the previous designs.

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